REMARKS

Prior to the present amendment and response, claims 1-8, 10-15, and 17-20 were pending in the present application. By the present amendment and response, claims 10, 15, and 17 have been amended to overcome the Examiner's objections. Claims 1-8, 10-15, and 17-20 remain in the present application. According to the Examiner's comments on pages 10 and 11 of the Office Action dated April 5, 2005, amended claims 15 and 17 and claims 18-20 are now in condition for allowance. Reconsideration and allowance of outstanding claims 1-8 and 10-14 in view of the above amendments and the following remarks are requested.

A. Objection to Claims 15 and 17-20

The Examiner has objected to claim 15 as containing an informality. Applicant has amended claim 15 and respectfully requests that the objection to claims 15 and 17-20 be withdrawn.

B. Rejection of Claims 10 and 17 under 35 USC §112, second paragraph

The Examiner has rejected claims 10 and 17 under 35 USC §112, second paragraph. Applicant has amended claims 10 and 17 and submits that the requirements of 35 USC §112, second paragraph, have been met.

C. **Double Patenting Rejections of Claims 1-8 and 10**

The Examiner has rejected claims 1-8 and 10 under the judicially created doctrine of obviousness-type double patenting over co-pending application number 10/637,146. Applicant has hereby concurrently filed a terminal disclaimer. As such, Applicant respectfully submits that the Examiner's obviousness-type double patenting rejection should now be withdrawn.

D. **Rejection of Claims 1-7 under 35 USC §103(a)**

The Examiner has rejected claims 1-7 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,566,954 B2 to Naoyuki Miyazawa (hereinafter "Miyazawa"). For the reasons discussed below, Applicant respectfully submits that independent claim 1 is patentably distinguishable over Miyazawa.

The present invention, as defined by independent claim 1, recites, among other things, a bias control circuit for a bias circuit, where the bias control circuit includes means for receiving a control voltage and means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage, where the equivalent resistance is established between a first node and a reference voltage. As disclosed in the present application, according to one embodiment, a bias control circuit includes a bias control transistor having a base coupled to a control voltage, a collector coupled to a bias circuit by a first resistor and coupled to ground by a second resistor, and an emitter coupled to ground by a third resistor.

As disclosed in the present application, the control circuit receives the control voltage and provides a reference resistance corresponding to an equivalent resistance between the first node and ground. As disclosed in the present application, the equivalent resistance controls the bias circuit, which in turn controls a quiescent current of an amplifier transistor. As disclosed in the present application, the first resistor (e.g. resistor 142 in Figure 1) establishes the primary resistance of the equivalent resistance for high mode operation, and the second resistor (e.g. resistor 144 in Figure 1) establishes the primary resistance of the equivalent resistance for low mode operation. As disclosed in the present application, due to the particular arrangement of the control circuit and the bias circuit, significantly improved analog control over the base voltage of the amplifier transistor by the control circuit is achieved, such that continuous quiescent current transition from a very low power level can be provided, which advantageously results in significant current savings. Also, since the control circuit is based on bipolar technology, the control circuit may be integrated in to the same die as the bias circuit and amplifier transistor, advantageously resulting in substantial cost savings and significantly reduced device size.

In contrast to the present invention as defined by independent claim 1, Miyazawa does not teach, disclose, or suggest a bias control circuit for a bias circuit, where the bias control circuit includes means for receiving a control voltage and means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage, where the equivalent resistance is established between a first node and a

reference voltage. Miyazawa specifically discloses high frequency amplifier bias circuit ("bias circuit") 2 coupled to transistor 21, which is an amplifier. See, for example, column 5, lines 6-19 and Figure 2 of Miyazawa. In Miyazawa, bias circuit 2 includes transistors 22, 23, 24, and 26, resistor 29, which couples the base of transistor 23 and the emitter of transistor 24 to ground, and resistor 27, which couples control input terminal 28 to the bases of transistors 22 and 24 and the collector of transistor 23. See, for example, column 5, lines 6-41 and Figure 2 of Miyazawa.

In Miyazawa, a stable bias electric current of transistor 21 (i.e. an amplifier) is obtained with respect to fluctuations in a control input voltage, which is applied to control input terminal 28. However, Miyazawa fails to teach, disclose, or remotely suggest a bias control circuit for a bias circuit, where the bias control circuit includes means for receiving a control voltage and means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage, where the equivalent resistance is established between a first node and a reference voltage, as specified in independent claim 1. In fact, Miyazawa fails to teach, disclose, or remotely suggest a bias control circuit for a bias circuit. Furthermore, Miyazawa provides no motivation for providing a bias control circuit for a bias circuit, where the bias control circuit receives a control voltage and provides a means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage.

On page 7 of the Office Action dated April 5, 2004, the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art to replace bias control circuit

(resistor) 29 of Miyazawa with at least one (bipolar) transistor receiving a control voltage to effectively function as a variable resistance within the circuit." In the above statement, the Examiner proposes to modify Yamamoto by replacing a single resistor (i.e. resistor 29), which the Examiner refers to as a "bias control circuit," with at least one transistor receiving a control voltage to effectively function as a variable resistance within the circuit. However, the Examiner has not provided any motivation as disclosed in Miyazawa or in the art for the Examiner's proposed modification of Miyazawa. Miyazawa is directed to providing an amplifier which is stable with respect to changes in temperature such that the amplifier can be directly controlled by the output signal of a digital logic circuit. See, for example, Miyazawa, column 6, lines 53-59.

In contrast, as disclosed in the present application, the present invention achieves a continuous quiescent current transition from a very low power level of an amplifier transistor by providing a bias control circuit for a bias circuit, where the bias control circuit receives a control voltage and provides a means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage. Thus, Applicant respectfully submits that the reason, suggestion, and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Applicant's disclosure.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not taught, disclosed, or suggested by Miyazawa. Thus, independent claim 1 is patentably distinguishable over Miyazawa. As

such, claims 2-7 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Miyazawa for at least the reasons presented above and also for additional limitations contained in each dependent claim.

E. Further Rejection of Claims 1-7 under 35 USC §103(a)

The Examiner has further rejected claims 1-7 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,043,714 to Yamamoto et al. (hereinafter "Yamamoto"). For the reasons discussed below, Applicant respectfully submits that independent claim 1 is patentably distinguishable over Yamamoto.

In contrast to the present invention as defined by independent claim 1, Yamamoto does not teach, disclose, or suggest a bias control circuit for a bias circuit, where the bias control circuit includes means for receiving a control voltage and means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage, where the equivalent resistance is established between a first node and a reference voltage. Yamamoto specifically discloses power amplifier 101 including bias circuit 101a, which includes first and second Si bipolar transistors Tr1 and Tr3 and HBT (heterojunction bipolar transistor) Tr2, and amplifier stage 101b, which includes HBT TrA. See, for example, column 8, lines 14-29 and Figure 2 of Yamamoto. However, Yamamoto fails to teach, disclose, or remotely suggest a bias control circuit including means for receiving a control voltage and means for actively adjusting an equivalent resistance of the bias control circuit responsive to the control voltage, where the

equivalent resistance is established between a first node and a reference voltage, as specified in independent claim 1.

Yamamoto discloses resistor R3, which couples the emitter of second Si bipolar transistor Tr3 and one terminal of resistor R4 to ground. See, for example, Figure 2 and related text of Yamamoto. On page 9 of the Office Action dated April 5, 2005, the Examiner states that "[i]t would have been obvious to one of ordinary skill in the art to replace bias control circuit (resistor) R3 of Yamamoto with at least one (bipolar) transistor receiving a control voltage to effectively function as a variable resistance within the circuit." As stated above, the Examiner proposes to modify Yamamoto by replacing a single resistor (i.e. resistor R3), which the Examiner refers to as a "bias control circuit," with at least one transistor receiving a control voltage to effectively function as a variable resistance within the circuit. However, the Examiner has failed to provide any motivation as disclosed in Yamamoto or in the art for the Examiner's proposed modification of Yamamoto. Thus, Applicant respectfully submits that the reason, suggestion, and motivation for the modification proposed by the Examiner is impermissible hindsight reconstruction given the benefit of the Applicant's disclosure.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claim 1, is not taught, disclosed, or suggested by Yamamoto. Thus, independent claim 1 is patentably distinguishable over Yamamoto. As such, claims 2-7 depending from independent claim 1 are, *a fortiori*, also patentably

distinguishable over Yamamoto for at least the reasons presented above and also for additional limitations contained in each dependent claim.

F. **Conclusion**

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 8 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-8 and 10-14 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of outstanding claims 1-8 and 10-14 and an early Notice of Allowance directed to all claims 1-8, 10-15, and 17-20 remaining in the present application are respectfully requested.

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Respectfully Submitted,
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